EXAMINER'S AMENDMENT

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

2. Authorization for this examiner's amendment was given in a telephone interview with Timonthy Boller (Reg No. 47,435) on June 23, 2009.

3. The claims have been amended as follows:

a. Claim 1: replace claim 1 with the following:

1. A process for executing programs on at least one processor having a given instruction set architecture, the process comprising the operations of:

compiling the program to be executed and translating said program into native instructions of said instruction set architecture, organizing the instructions deriving from the translation of said program into respective bundles arranged in an order of successive bundles, each bundle grouping together instructions adapted to be executed in parallel by said at least one processor, each bundle having a determined priority for execution by said at least one processor;

separating said bundles of instructions into respective sub-bundles by detecting a value of a binary symbol encoded in one of the instructions deriving from the translation of the program to be executed of the respective bundle, said sub-bundles identifying a

first set of instructions, which must be executed before the instructions belonging to the next bundle of said order, and a second set of instructions that can be executed both before and in parallel with respect to the instructions belonging to said next bundle of said order, it being possible for at least said second set of instructions to be a null set;

defining a sequence of execution of the instructions of said sub-bundles in successive operating cycles of said at least one processor based on said determined priority carried by a designated number of bits encoded into each instruction, while preventing, in assigning each sub-bundle to an operating cycle of the processor, simultaneous assignment, to the same operating cycle, of two sub-bundles corresponding to instructions belonging to a first set of two successive bundles of said order; and

executing said instructions on at least one said processor respecting said execution sequence.

b. Claim 12: replace claim 12 with the following:

12. A process of executing programs on a system having a plurality of processors comprising:

compiling the program to be executed;

translating said program into instruction sets;

organizing said instruction sets into respective groups, each group having a predetermined priority for execution in a given processor of said plurality;

separating each group of instructions into a respective first sub-bundle of instructions which must be executed before the instructions belonging to the next group,

and a respective second sub-bundle of instructions that can be executed before or in parallel with respect to the instructions belonging to said next group, it being possible for at least said second sub-bundle of instructions to be a null set;

encoding said instructions for execution on said processors;

providing in each encoded instruction a designated number of initial bits identifying said predetermined priority of the instruction set; and

wherein the execution of programs comprises directing of the sub-bundled instruction sets to said processors of said plurality according to the priority bits encoded into the said instruction set.

c. Claim 13 is cancelled.

d. Claim 16: replace claim 16 with the following:

16. A system comprising:

a plurality of processors coupled for receiving instruction sets, each instruction set containing one or more instructions; and

a first processor of the plurality coupled to an instruction stream and capable of directing said instruction sets to each of the processors of said plurality for execution including organizing said instruction sets into respective bundles arranged in an order of successive bundles, each bundle having a determined priority for execution in a given processor of said plurality, separating said bundles of instructions into respective sub-bundles by detecting a value of a binary symbol encoded in one of the instructions

deriving from a translation of a program to be executed of the respective bundle, said sub-bundles identifying a first set of instructions, which must be executed before the instructions belonging to the next bundle of said order, and a second set of instructions that can be executed both before and in parallel with respect to the instructions belonging to said next bundle of said order, it being possible for at least said second set of instructions to be a null set;

said first processor configured to direct the sub-bundled instructions sets to the processors of said plurality based on priority values carried by a designated number of bits encoded into each instruction.

Reasons for Allowance

4. The following is an examiner's statement of reasons for allowance: the prior art of record fails to teach or suggest the claimed invention. Specifically, the prior art of record, Menezes and Tulia, fail to teach sub-bundles identifying a first set of instructions, which must be executed before the instructions belonging to the next bundle of said order, and a second set of instructions that can be executed both before and in parallel with respect to the instructions belonging to said next bundle of said order, and the sub-bundled instructions are further directed to a processor based on priority values carried by a designated number of bits encoded into each instruction.

5. Any comment considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue

fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jue S. Wang whose telephone number is (571) 270-1655. The examiner can normally be reached on M-Th 7:30 am - 5:00pm (EST).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lewis Bullock can be reached on 571-272-3759. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Lewis A. Bullock, Jr./
Supervisory Patent Examiner, Art Unit 2193

/Jue S Wang/
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